IN THE CLAIMS:

Claim 1 (Withdrawn): A semiconductor device comprising:

a semiconductor substrate including an element partitioning trench and a mask aligning trench;

a first insulation deposited in the element partitioning trench; and

a second insulation partially deposited in the mask aligning trench formed from the same substance as the first insulation.

Claim 2 (Withdrawn): The semiconductor device according to claim 1, wherein the mask aligning trench has a upper edge, and wherein an upper surface of the second insulation defines a step with the upper edge.

3. (Currently amended): A method for manufacturing a semiconductor device, the method comprising:

forming a film on an upper surface of a semiconductor substrate;

forming an element partitioning trench and a mask aligning trench in [[a]] the semiconductor substrate;

simultaneously depositing an insulation in the element partitioning trench and the mask aligning trench by a chemical vapor deposition process consisting of high density plasma chemical vapor deposition, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

applying a protective mask on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench;

etching the insulation deposited in the mask aligning trench to remove some of the insulation while the insulation deposited in the element partitioning trench is covered by the protective mask so that the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate; ~~and~~

removing the protective mask;

flattening an upper surface of the semiconductor device; and

selectively removing the film so that a step is formed between the upper surface of the semiconductor substrate and [[an]] the upper surface of the ~~first~~ insulation deposited in the element partitioning trench.

Claim 4 (Original): The method according to claim 3, wherein the step of forming the element partitioning trench and the mask aligning trench includes:

forming a coating on the semiconductor substrate,

wherein the coating has a pattern of openings corresponding to the element partitioning trench and the mark aligning trench; and

etching the semiconductor substrate using the coating as a mask to form the element partitioning trench and the mask aligning trench, wherein the insulation depositing step includes depositing the insulation without removing the coating.

Claim 5 (Original): The method according to claim 4, wherein the flattening step is performed through rotary grinding, and the coating functions as a stopper.

Claim 6 (Original): The method according to claim 5, wherein the semiconductor substrate is a silicon substrate, the insulation is formed from silicon oxide, and the coating is formed from silicon nitride, the method further comprising the step of forming a silicon oxide film on the semiconductor substrate prior to the formation of the element partitioning trench and mask aligning trench, wherein the coating is formed on the silicon oxide film.

7. (Currently amended): A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a silicon oxide film on an upper surface of a semiconductor substrate;

forming a silicon nitride film on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film;

forming an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths;

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively by a chemical vapor deposition process consisting of high density plasma chemical vapor

deposition, wherein no other insulation has been deposited by a plasma process in the trenches prior to the insulation being deposited;

coating the first insulation with a protective mask to fully cover the element partitioning trench;

etching the second insulation while the first insulation is covered by the protective mask so that a first step is formed between [[an]] the upper surface of the semiconductor substrate and an upper surface of the second insulation;

removing the protective mask;

flattening an upper surface of the semiconductor device; and

selectively removing the silicon nitride film and the silicon oxide film so that a second step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation.

Claim 8 (Original): The method according to claim 7, wherein the first insulation and the second insulation are made of the same material.

9. (Currently amended): A method for manufacturing a semiconductor device, the method comprising:

forming a film on an upper surface of a semiconductor substrate;

forming an element partitioning trench and a mask aligning trench in [[a]] the semiconductor substrate;

simultaneously depositing an insulation in the element partitioning trench and the mask aligning trench by a chemical vapor deposition process consisting of high density plasma chemical vapor deposition, the insulation directly contacting the semiconductor substrate;

applying a protective mask on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench;

etching the insulation deposited in the mask aligning trench to remove some of the insulation while the insulation deposited in the element partitioning trench is covered by the protective mask so that the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate;

removing the protective mask;

flattening an upper surface of the semiconductor device; and

selectively removing the film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the ~~first~~ insulation in the element partitioning trench.

10. (Currently amended): A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a silicon oxide film on an upper surface of a semiconductor substrate;

forming a silicon nitride film on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film;

forming, an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths;

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively by a chemical vapor deposition process consisting of high density plasma chemical vapor deposition, the first layer of insulation and the second layer of insulation directly contacting the semiconductor substrate;

coating the first insulation with a protective mask to fully cover the element partitioning trench;

etching the second insulation while the first insulation is covered by the protective mask so that a first step is formed between an upper surface of the semiconductor substrate and an upper surface of the second insulation;

removing the protective mask; and

selectively removing the silicon nitride film and the silicon oxide film so that a second step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation.

11. (New): The method according to claim 3, wherein height difference between the upper surface of the insulation deposited in the mask aligning trench and the upper surface

located lower than the upper surface of the semiconductor substrate is adjustable by said etching the insulation deposited in the mask aligning trench.

12. (New): The method according to claim 3, further comprising:

patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning the conductive film.

13. (New): The method according to claim 7, wherein height of the first step is adjustable by said etching the second insulation.

14. (New): The method according to claim 7 further comprising:

patterning a conductive film on the semiconductor substrate, wherein the height of the second step at the time of removing the silicon nitride film is adjusted to a predetermined height that is equal to a depth etched during said removing the silicon oxide film and said patterning the conductive film.

15. (New): The method according to claim 9, wherein height difference between the upper surface of the insulation deposited in the mask aligning trench and the upper surface located lower than the upper surface of the semiconductor substrate is adjustable by said etching the insulation deposited in the mask aligning trench.

16. (New): The method according to claim 9, further comprising:

patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of selectively removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning the conductive film.

17. (New): The method according to claim 10, wherein height of the first step is adjustable by said etching the second insulation.

18. (New): The method according to claim 10, further comprising:

patterning a conductive film on the semiconductor substrate, wherein the height of the second step at the time of removing the silicon nitride film is adjusted to a predetermined height that is equal to a depth etched during said removing the silicon oxide film and said patterning the conductive film.